

R A Q ' s

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Tick-Tock, Tick-Tock

Q. *My clock is accurate to 1 ppm—what could possibly need improvement?*

A. The phase noise or jitter. The performance of any ac sampling system is critically dependent on the use of a sampling clock with adequately low jitter.

A quarter of a century ago I was technical advisor to a Parliamentary Committee on CB Radio. We

met at Westminster Hall in the Houses of Parliament in London, almost directly under Big Ben, whose chimes punctuated our deliberations. I frequently used Big Ben as an example when explaining the importance of various features of clocks and oscillators.

In a sampled data system, a changing signal is sampled at regular intervals and the signal is processed by performing calculations on the samples. If an oscillator has jitter, the clock edges occur earlier or later than they would in a jitter-free clock. The frequency accuracy is unaffected, only the exact timing of individual transitions varies.

If an edge comes early, the signal being sampled will not yet have reached its correct value, and if it comes late, the signal will have moved on—so to achieve accuracy in a sampled system it is important to have adequately low jitter on the system clock. In fact, frequency accuracy is often far less important. Obviously, the faster the sampled signal is changing, the greater the error will be for a given amount of jitter. The clock frequency is irrelevant—it is the frequency of the analog signal being sampled (in the case of the ADC) or signal being synthesized (in the case



of the DAC) that matters.

Although the problem can be significant at quite modest signal frequencies (I have memories of digital audio systems with performance devastated by inappropriate clock oscillators—one a 555 timer,

another an interrupt-driven microprocessor) it becomes critical in modern digital radios using IF sampling at signal frequencies of tens or hundreds of MHz. To give numbers, a perfect ADC (no imperfections of any sort) working with a 100 MHz signal and a clock with one picosecond ($1\text{E}-12$ seconds) rms jitter cannot achieve a resolution greater than 10 bits.

Links to information on the relevant formula, low noise clock circuits, and circuit techniques that ensure a low clock jitter signal is not degraded before it reaches the circuits it drives, are on the website below. A simple illustration of the difference between clock accuracy and clock jitter is to consider what would happen if Big Ben's hands always pointed to the exact time, but the chime occurred randomly up to five minutes early or late.

To learn more on accurately timing clocks,

Go to:

<http://rbi.ims.ca/5696-105>



Contributing Writer
James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

raq@reedbusiness.com

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