

An Auto-Powered Semi 'break-in' Keyer

By James Bryant,
G4CLF, MIERE.

With the recent growth in the use of CW at VHF and UHF there is a need for a simple circuit which can provide 'break-in' facilities for VHF/UHF transceivers which do not have it.

agc. With semi break-in keying the receiver switches off when the key closes and remains off until the key has been open for a predetermined period — normally of the order of a few

Most modern HF transceivers are equipped with semi break-in keying as standard — most VHF transceivers are not.

In a transceiver equipped with break-in keying the receiver is active whenever the key is not closed — the operator can thus listen for responses in the short intervals between dots and dashes. The design of receivers capable of working in this way is very demanding since they must respond to weak signals within milliseconds of the transmitter ceasing to generate very high powers at the same frequency — this places great constraints on the strong-signal performance and the operation of the

hundred milliseconds — the demands on receiver design are correspondingly less stringent. The operator can still monitor while transmitting but must make an infinitesimal pause to do so. Transceivers fitted with semi break-in keying normally use the VOX (voice-operated transmit/receive) circuitry to perform the function.

The present design does not use VOX circuitry but instead uses a CMOS logic arrangement driving a VMOS output transistor to switch the PTT (push to talk) line of the

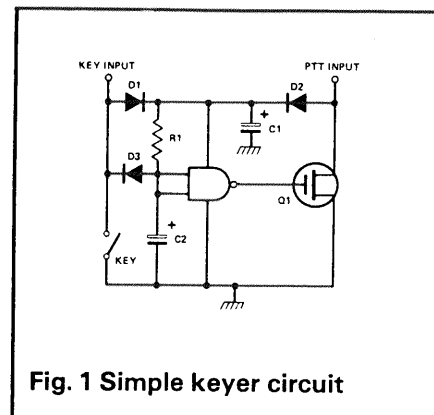


Fig. 1 Simple keyer circuit

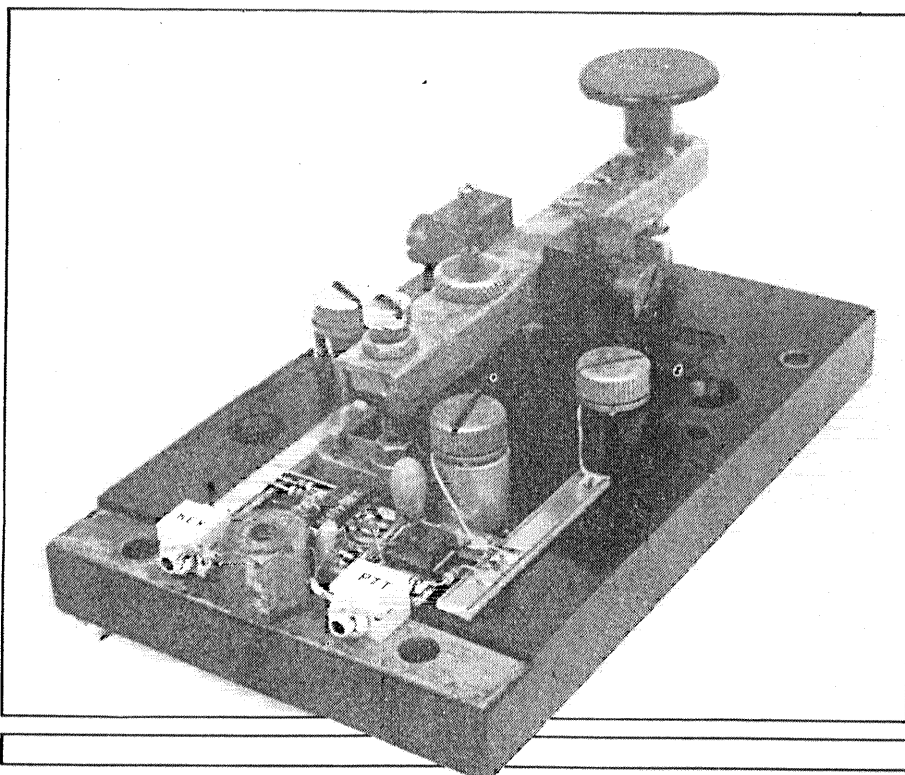
transceiver. The use of MOS allows the keyer to run from the small current which may be taken from the PTT and key lines without keying and the circuit needs no other power supply. This is particularly convenient during contests since keyer batteries are notorious for failing when no replacements are available.

The Circuit

A circuit which will perform the function is shown in Fig 1. It consists of a single schmitt input CMOS gate and an N-Channel VMOS transistor. There are also three diodes, two capacitors and a resistor (which may be variable).

Its operation is simple — when first powered the capacitor C1 is charged via D1 and/or D2 (whichever is at a higher potential) and then this capacitor powers the CMOS circuit, which draws well under 1 microamp of current from its supply. When the key is open C2 is charged, the input to the gate is at logic 1 and hence its output and the gate of Q1 are low so that Q1 is turned off.

When the key is closed C2 at once discharges through D3 and the output of the gate rises, turning on Q1, which grounds the PTT line, switching the transceiver to 'TRANSMIT'. Being a VMOS device Q1 draws no gate



current so C1 holds charge for many seconds.

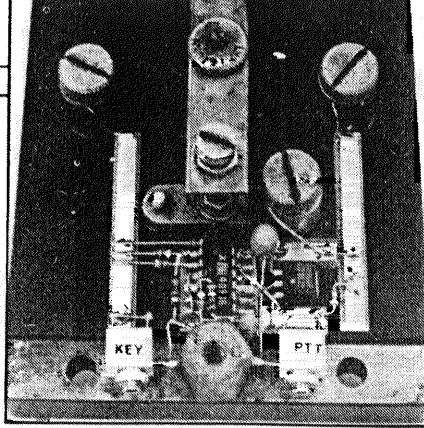
Before C1 can discharge the key will be opened and it will recover charge from the key line of the transceiver via D1. C2 will start to charge slowly through R1 but Q1 will remain on until the voltage on C2 reaches the threshold of the gate's switching action (taking several hundred mSec, depending on the value of R1). During normal transmission the key will close again before this can happen and C2 will be discharged. Thus the PTT line will be grounded steadily during CW transmission.

If the key remains open for more than the time taken for C2 to charge to the gate's switching threshold the gate will change state, Q1 will be turned off, and the PTT line will revert to 'RECEIVE'.

A drawback of this circuit is that as well as powering the gate, C1 is also discharged through R1. Since CMOS schmitt input gates normally come in DIL packages of four (4093) or six (40106) it costs nothing to use a few extra gates to reduce the current drawn from C1. The final circuit, shown in Fig 2, does this.

The final circuit uses two more CMOS gates to isolate the timing circuitry from the key and also requires two diodes and a resistor (D4, D5 & R2) to keep the logic voltages within the permitted range. R1 is connected in parallel with D3 instead of to the "power line" and an extra diode is incorporated to protect Q1 if the system is used with an inductive load (such as a relay) in the PTT line.

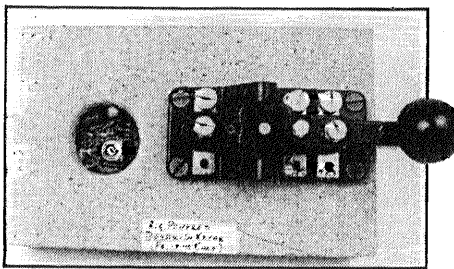
This circuit uses three gates so that a 4093 quad schmitt NAND which contains four gates is ideal for the application. The pin numbers indicated apply to this part although any other CMOS schmitt input gates (such as the 40106) could equally well be used. The capacitors C1 and C2 should be low-leakage types so it is



Construction of the G4CLF keyer

worthwhile using bead tantalum types rather than aluminium — the extra cost is only pence. The diodes are silicon small-signal types such as the 1N914 or 1N4148 and are quite non-critical, and the VMOS transistor, Q1, is an N-channel type such as the Siliconix VN66AF.

The circuit may be constructed in any suitable manner — it is very simple and component placing is not at all critical. The author's prototype uses Wainwright Minimount PC breadboarding strip mounted on the base of the morse key itself.



Another variant of the G4CLF keyer.

Connection

Before connecting the keyer to a transceiver several measurements should be made. The voltage and current available at both the PTT and the key connections should be checked by connecting first a high resistance voltmeter and then a milliammeter between these points and ground (note that the connection

of the millimeter will cause the rig to transmit so a suitable power source and antenna should be connected).

This circuit will work with PTT and key line voltages of between 5 and 18 volts positive and will NOT work with transceivers having negative PTT or key lines. If the PTT line has a voltage above 18 the keyer must be modified by removing D2 (which causes the keyer to be powered from the key line only) and replacing D6 with a higher voltage part. Above 60 volts the VMOS device must also be replaced by one capable of withstanding the necessary voltage. If the key line has a voltage of over 18 volts the keyer cannot take its power from the key line but must be battery powered by a PP3 battery connected in parallel with C1. In addition, D5 must be removed, the grounded end of R2 connected to the battery positive and D4 replaced with a device capable of withstanding the necessary reverse voltage.

Provided the PTT and key currents are more than 100 microamps and less than 250 milliamps the circuit should work correctly (PTT currents of over 250 mA may be accommodated by using a higher powered VMOS device).

The keyer is connected to the transceiver by connecting the PTT and key lines to the appropriate sockets of the transceiver — when the key is closed (provided the transceiver is set to 'CW') the rig will switch to 'TRANSMIT' and remain that way until the key has been open continuously for a time set by R1 and C2. In the prototype R1 is 220K and C2 is 0.47 uF and the delay is about half a second but variation in the threshold voltages of the CMOS used may change this quite widely and R1, and even C2, may need to be changed to achieve the correct delay. R1 should never be less than 180K but may be as high as 4.7M.

This keyer has been in use with the author's FT290 for over six months and has proved very useful. It has been widely copied.

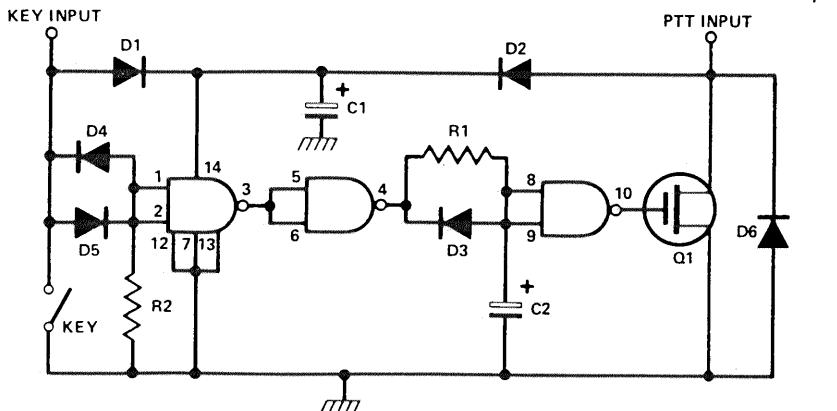


Fig. 2 Final version using 4093.

COMPONENTS LIST

- R1 220K (see text)
- R2 1M
- C1 100u 25V tant.
- C2 0.47u 16V tant.
- D1-6 1N914, 1N9148 (see text)
- Q1 VN66AF
- IC1 4093 CMOS